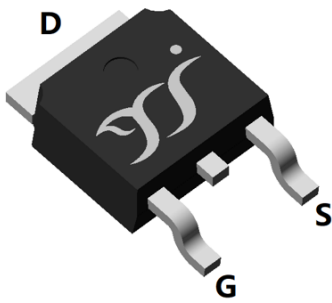
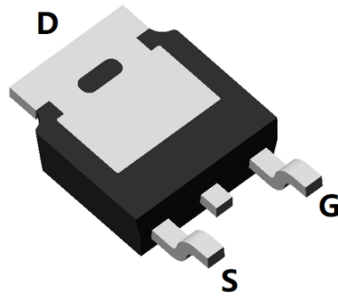


## N-Channel Enhancement Mode Field Effect Transistor

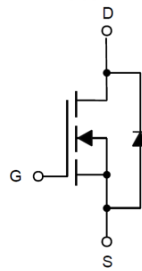


Top View



Bottom View

**TO-252**



### Product Summary

- $V_{DS}$  60V
- $I_D$  80A
- $R_{DS(ON)}$ ( at  $V_{GS}=10V$ ) <7.5 mohm
- $R_{DS(ON)}$ ( at  $V_{GS}=4.5V$ ) <9.5 mohm
- 100% EAS Tested
- 100%  $\nabla V_{DS}$  Tested

### General Description

- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low  $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

### Applications

- DC-DC Converters
- Power management functions
- Industrial and Motor Drive application

### ■ Absolute Maximum Ratings ( $T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		$V_{DS}$	60	V
Gate-source Voltage		$V_{GS}$	$\pm 20$	V
Drain Current (Silicon limited)	$T_C=25^\circ\text{C}$	$I_D$	80	A
	$T_C=100^\circ\text{C}$		50	
Pulsed Drain Current <sup>A</sup>		$I_{DM}$	240	A
Avalanche energy <sup>B</sup>		$E_{AS}$	150	mJ
Total Power Dissipation <sup>C</sup>	$T_C=25^\circ\text{C}$	$P_D$	78	W
	$T_C=100^\circ\text{C}$		31	
Junction and Storage Temperature Range		$T_J, T_{STG}$	-55~+150	$^\circ\text{C}$

### ■ Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient <sup>D</sup>	$t \leq 10\text{S}$	$R_{\theta JA}$	15	20	$^\circ\text{C/W}$
Thermal Resistance Junction-to-Ambient <sup>D</sup>	Steady-State		40	50	
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	1.3	1.6	

### ■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJD80G06C	F1/F2	YJD80G06C	2500	2500	25000	13" reel



# YJD80G06C

## ■ Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> =250μA	60			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V	T <sub>J</sub> =25°C		1	μA
			T <sub>J</sub> =55°C		5	
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V, V <sub>DS</sub> =0V			±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =250μA	1.2	1.7	2.5	V
Static Drain-Source On-Resistance	R <sub>Ds(ON)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> =20A		5.5	7.5	mΩ
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> =10A		6.9	9.5	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =20A, V <sub>GS</sub> =0V		0.85	1.3	V
Maximum Body-Diode Continuous Current	I <sub>S</sub>				80	A
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =35V, V <sub>GS</sub> =0V, f=1MHz		2000	2800	pF
Output Capacitance	C <sub>oss</sub>			390	600	
Reverse Transfer Capacitance	C <sub>rss</sub>			13	25	
Gate Resistance	R <sub>g</sub>	f=1MHz, Open drain		1.6	2.5	Ω
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub> (10V)	V <sub>DS</sub> =30V, I <sub>D</sub> =20A		34	50	nC
Total Gate Charge	Q <sub>g</sub> (4.5V)			15.8	25	
Gate-Source Charge	Q <sub>gs</sub>			7.8	15	
Gate-Drain Charge	Q <sub>gd</sub>			5.2	10	
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> =20A, di/dt=200A/us		36		
Reverse Recovery Time	t <sub>rr</sub>			27		
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =10V, V <sub>DD</sub> =30V, I <sub>D</sub> =12A R <sub>GEN</sub> =3Ω		10		ns
Turn-on Rise Time	t <sub>r</sub>			36		
Turn-off Delay Time	t <sub>D(off)</sub>			30		
Turn-off fall Time	t <sub>f</sub>			57		

A. Repetitive rating; pulse width limited by max. junction temperature.

B. V<sub>DD</sub>=50V, R<sub>G</sub>=25Ω, L=0.5mH, I<sub>AS</sub>=24.5A,.

C. Pd is based on max. junction temperature, using junction-case thermal resistance.

D. The value of R<sub>θJA</sub> is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub> =25°C. The Power dissipation P<sub>DSM</sub> is based on R<sub>θJA</sub> ≤ 10s and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.



## ■ Typical Performance Characteristics

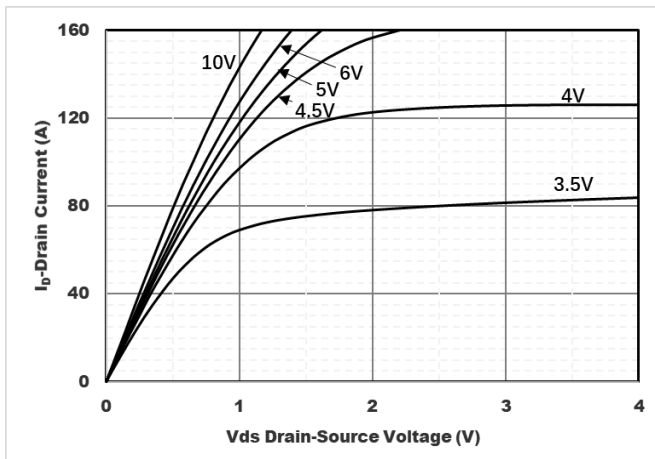


Figure1. Output Characteristics

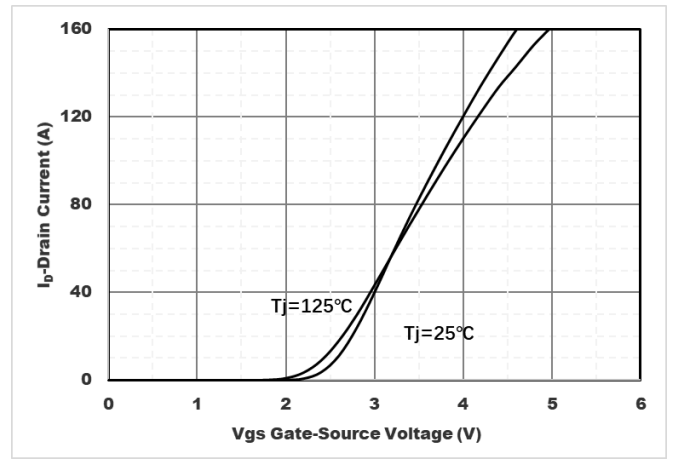


Figure2. Transfer Characteristics

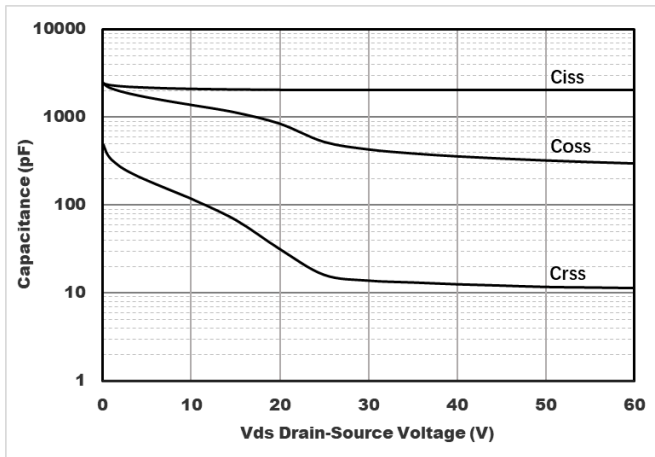


Figure3. Capacitance Characteristics

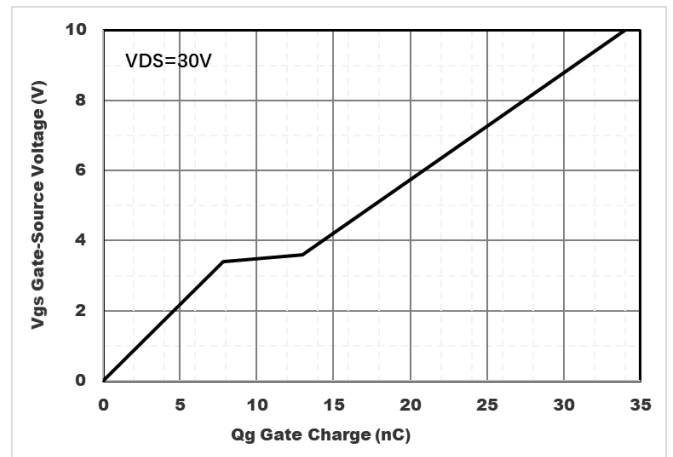


Figure4. Gate Charge

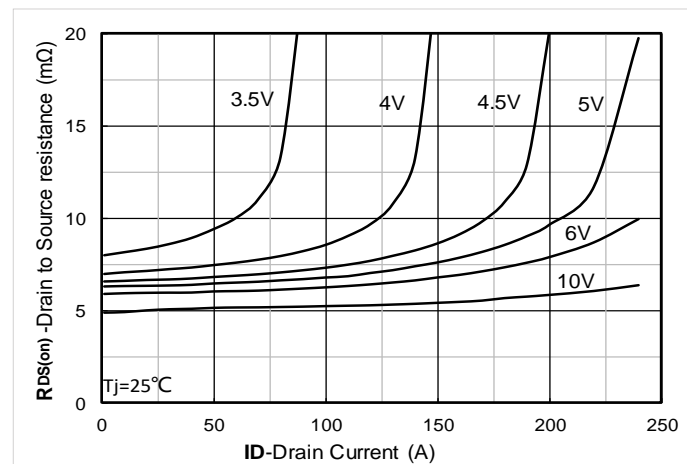


Figure5. Drain-Source on Resistance

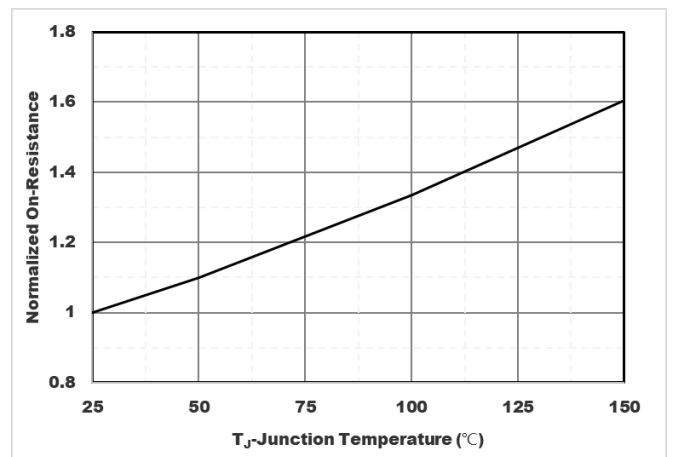


Figure6. Normalized On-Resistance



# YJD80G06C

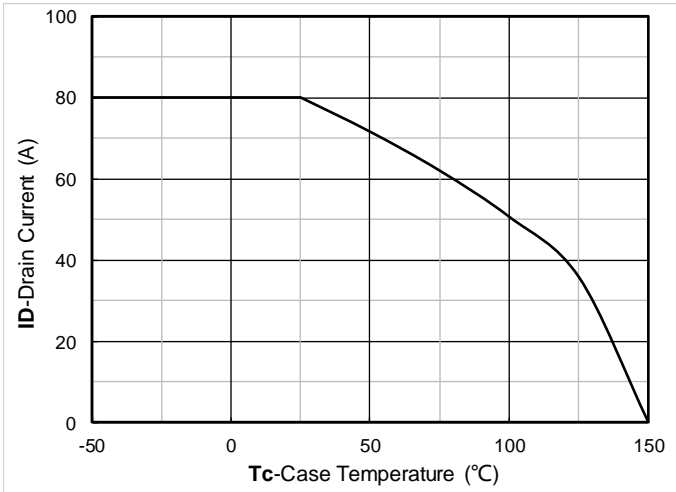


Figure7. Drain current

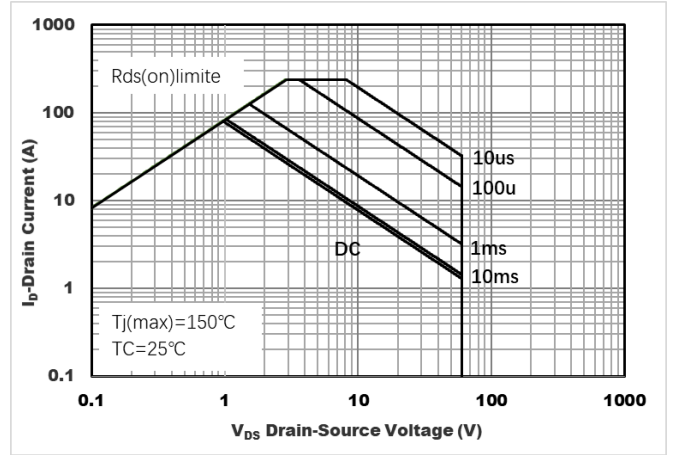


Figure8. Safe Operation Area

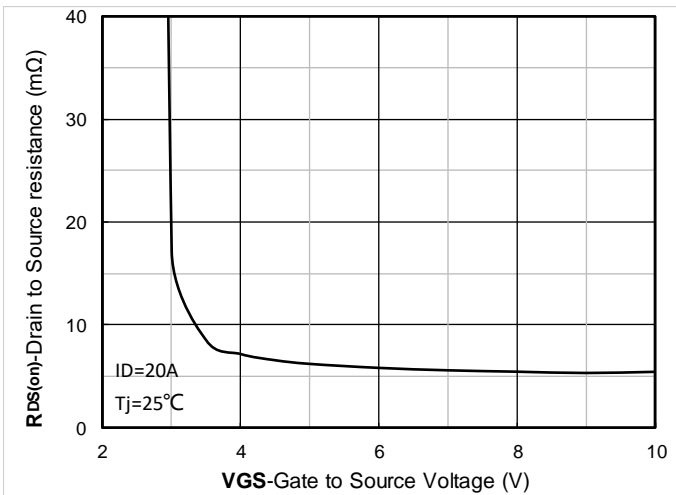


Figure 9. On-Resistance vs Gate to Source Voltage

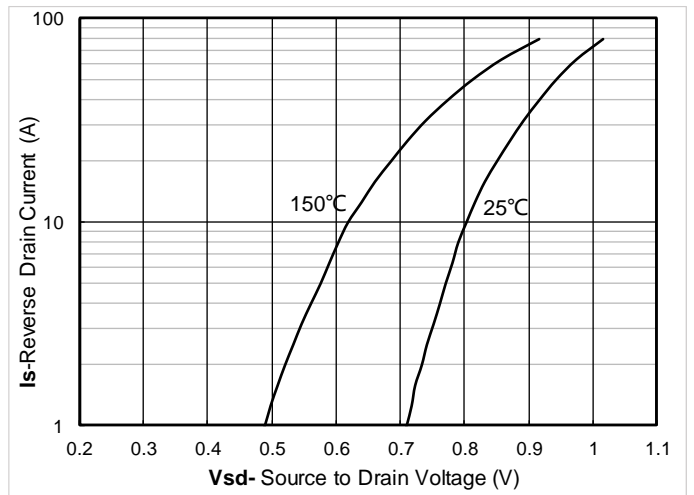


Figure 10. Forward characteristics of reverse diode

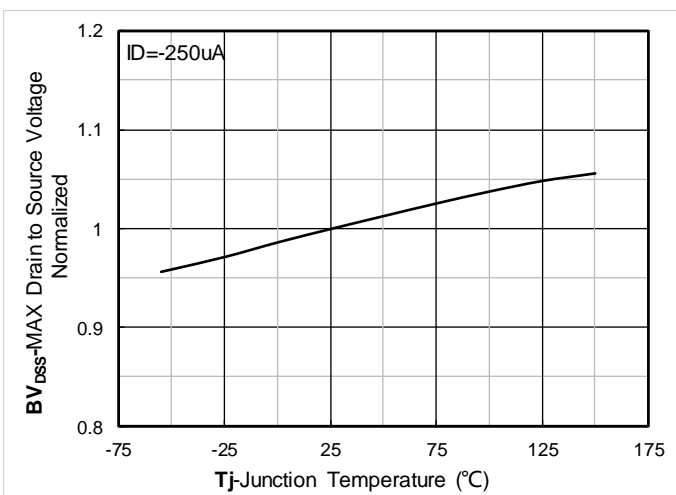


Figure11. Normalized breakdown voltage

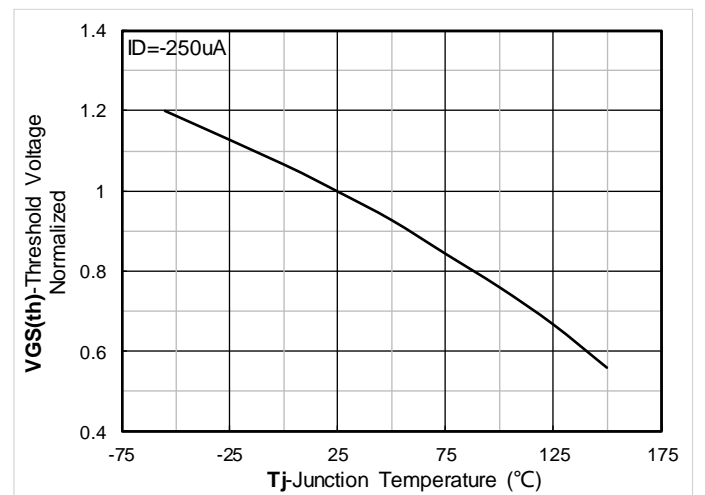


Figure 12. Normalized Threshold voltage

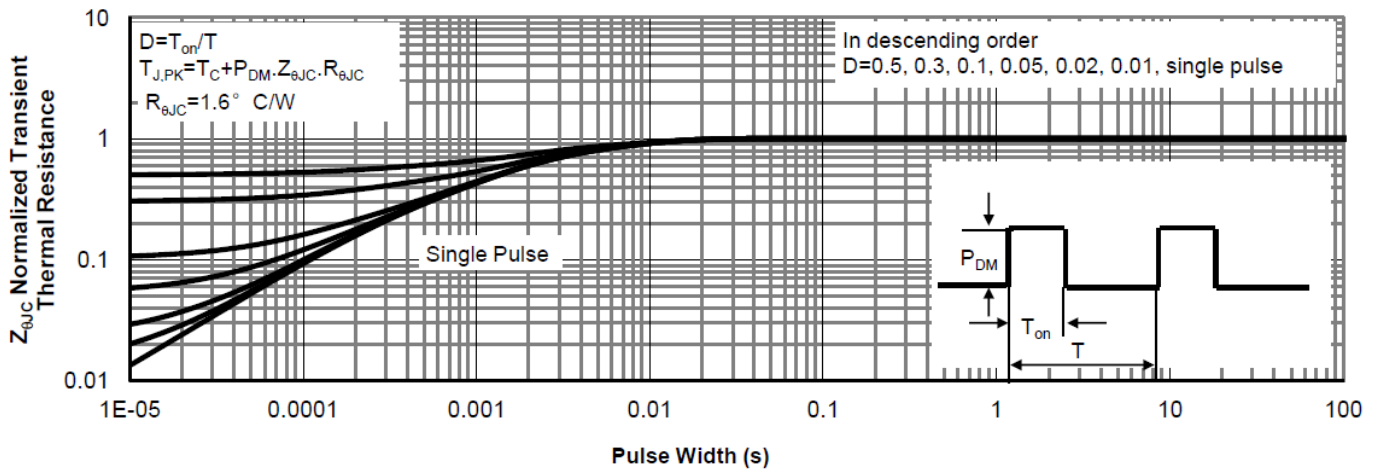
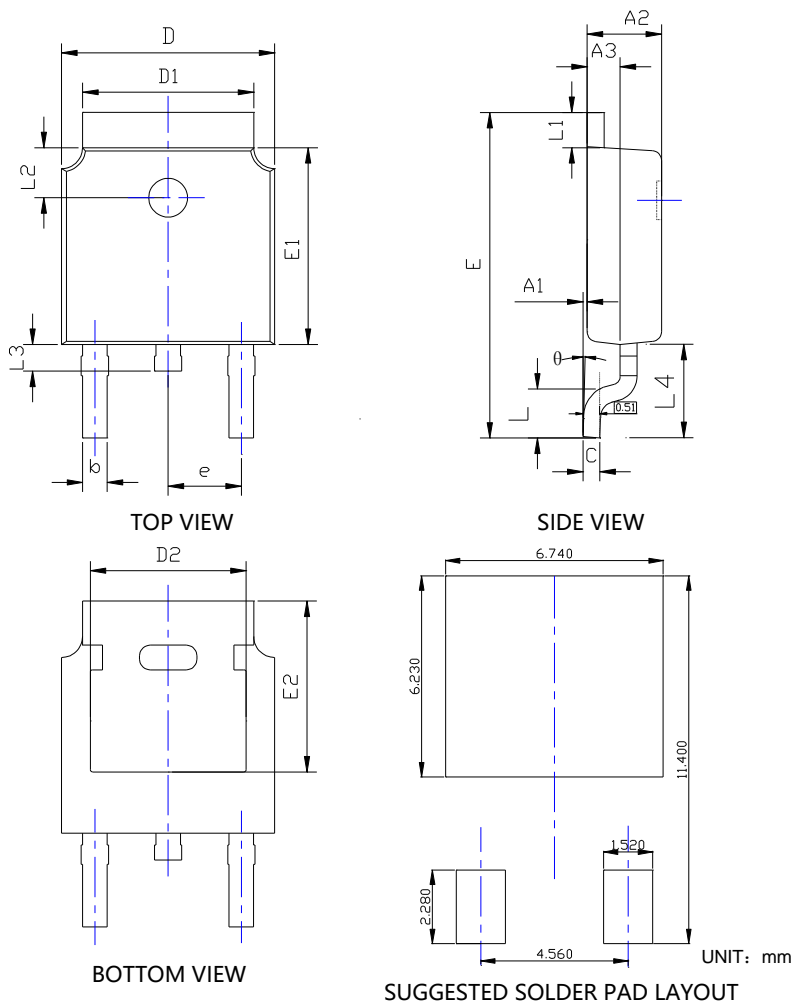


Figure13. Normalized Maximum Transient Thermal Impedance

## ■ TO-252-B Package information



SYMBOL	DIMENSIONS					
	INCHES			Millimeter		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A1	0.000	---	0.008	0.000	---	0.200
A2	0.087	0.091	0.094	2.200	2.300	2.400
A3	0.035	0.039	0.043	0.900	1.000	1.100
b	0.026	0.030	0.034	0.660	0.760	0.860
c	0.018	0.020	0.023	0.460	0.520	0.580
D	0.256	0.260	0.264	6.500	6.600	6.700
D1	0.203	0.209	0.215	5.150	5.300	5.450
D2	0.181	0.189	0.195	4.600	4.800	4.950
E	0.390	0.398	0.406	9.900	10.100	10.300
E1	0.236	0.240	0.244	6.000	6.100	6.200
E2	0.203	0.209	0.215	5.150	5.300	5.450
e	0.090BSC			2.286BSC		
L	0.049	0.059	0.069	1.250	1.500	1.750
L1	0.035	---	0.050	0.900	---	1.270
L2	0.055	---	0.075	1.400	---	1.900
L3	0.240	0.310	0.039	0.600	0.800	1.000
L4	0.114REF			2.900REF		
θ	0°	---	10°	0°	---	10°

**NOTE:**

- 1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
- 2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
- 3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.



## YJD80G06C

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