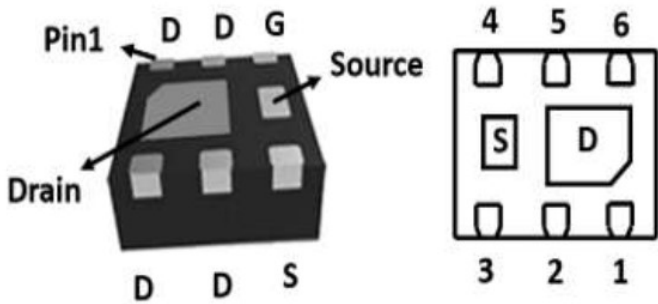
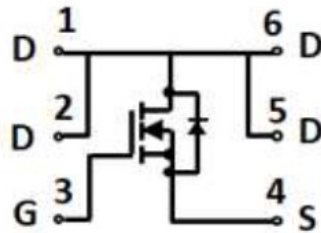


## N-Channel Enhancement Mode Field Effect Transistor



**DFN2x2-6L**



### Product Summary

- $V_{DS}$  30V
- $I_D$  13A
- $R_{DS(ON)}$  (at  $V_{GS}=10V$ ) < 12 mohm
- $R_{DS(ON)}$  (at  $V_{GS}=4.5V$ ) < 15 mohm

### General Description

- Trench Power LV MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low  $R_{DS(ON)}$

### Applications

- High current load applications
- Load switching
- Hard switched and high frequency circuits
- Uninterruptible power supply

### ■ Absolute Maximum Ratings ( $T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-source Voltage	$V_{DS}$	30	V
Gate-source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current	$I_D$	$T_C=25^\circ\text{C}$	13
		$T_C=100^\circ\text{C}$	8.0
Pulsed Drain Current <sup>A</sup>	$I_{DM}$	55	A
Total Power Dissipation	$P_D$	$T_C=25^\circ\text{C}$	2.9
		$T_C=100^\circ\text{C}$	1.2
Thermal Resistance Junction-to-Ambient <sup>B</sup>	$R_{\theta JA}$	43	$^\circ\text{C/W}$
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55~+150	$^\circ\text{C}$

### ■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJQ13N03A	F1	Q13N03	3000	30000	120000	7" reel



# YJQ13N03A

## ■ Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> =250μA	30			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V	T <sub>J</sub> =25°C		1	μA
			T <sub>J</sub> =55°C		5	
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V, V <sub>DS</sub> =0V			±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =250μA	1.0	1.5	2.5	V
Static Drain-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> =8A		7	12	mΩ
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> =5A		11	15	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =13A, V <sub>GS</sub> =0V			1.2	V
Maximum Body-Diode Continuous Current	I <sub>S</sub>				13	A
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V, f=1MHZ		1015		pF
Output Capacitance	C <sub>oss</sub>			201		
Reverse Transfer Capacitance	C <sub>rss</sub>			164		
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> =10V, V <sub>DS</sub> =20V, I <sub>D</sub> =20A		23.6		nC
Gate-Source Charge	Q <sub>gs</sub>			3.8		
Gate-Drain Charge	Q <sub>gd</sub>			7		
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> =15A, di/dt=100A/us		0.2		ns
Reverse Recovery Time	t <sub>rr</sub>			5		
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =10V, V <sub>DD</sub> =20V, I <sub>D</sub> =2A, R <sub>GEN</sub> =3Ω		7		ns
Turn-on Rise Time	t <sub>r</sub>			20		
Turn-off Delay Time	t <sub>D(off)</sub>			24		
Turn-off fall Time	t <sub>f</sub>			24		

A. Pulse Test: Pulse Width ≤ 300us, Duty cycle ≤ 2%.

B. R<sub>θJA</sub> is the sum of the junction-to-Case and Case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>θJC</sub> is guaranteed by design, while R<sub>θJA</sub> is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.



■ Typical Performance Characteristics

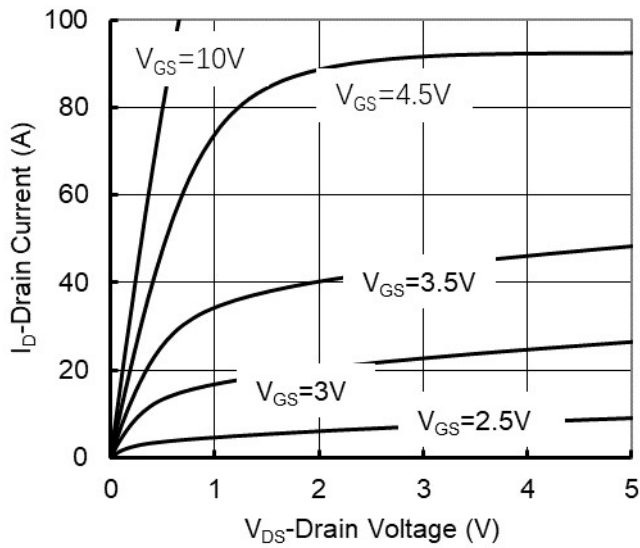


Figure1. Output Characteristics

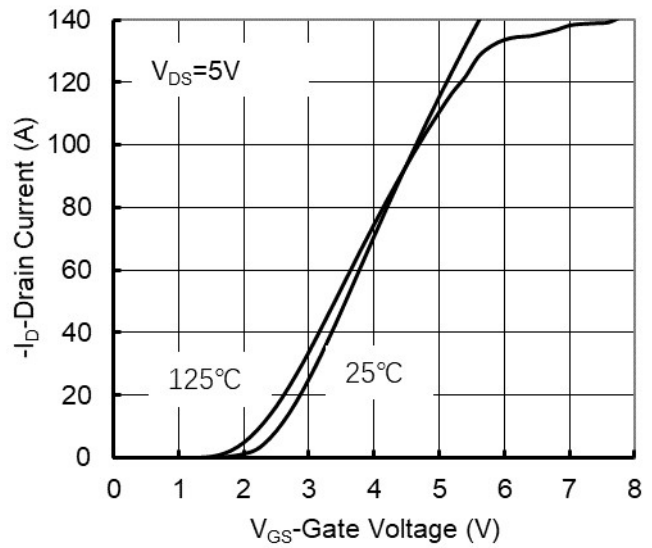


Figure2. Transfer Characteristics

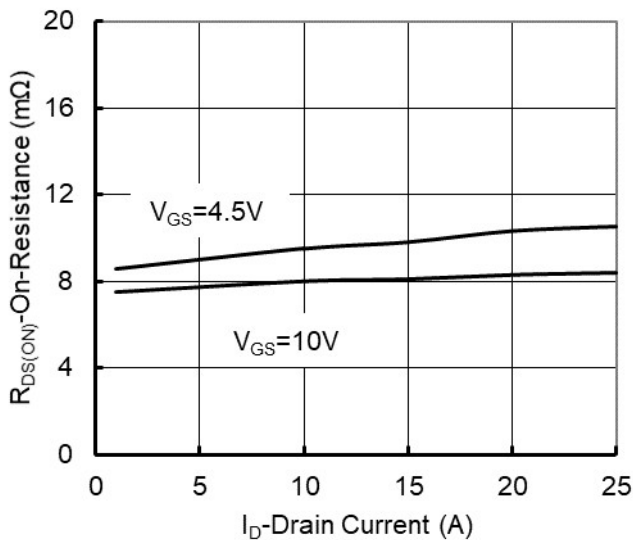


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

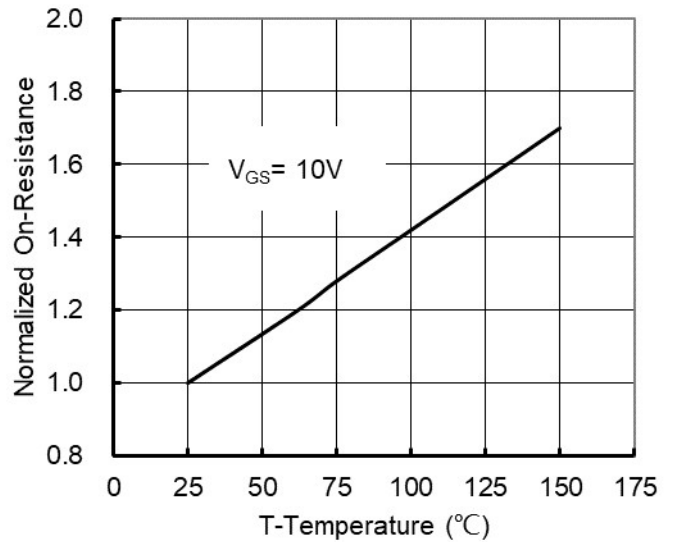


Figure 4: On-Resistance vs. Junction Temperature

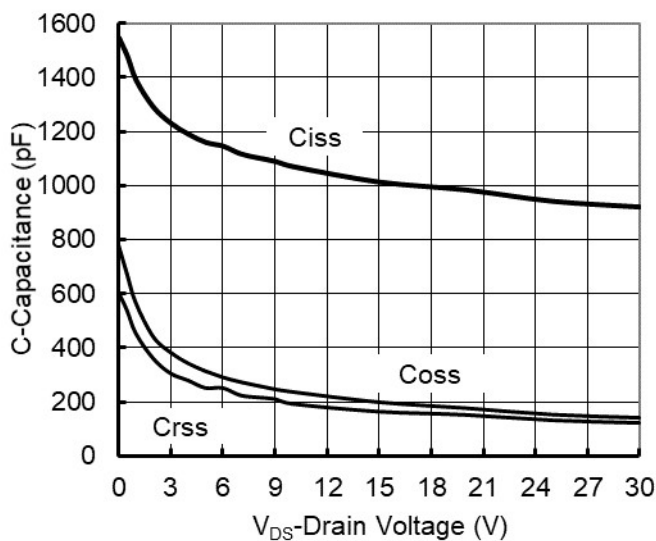


Figure5. Capacitance Characteristics

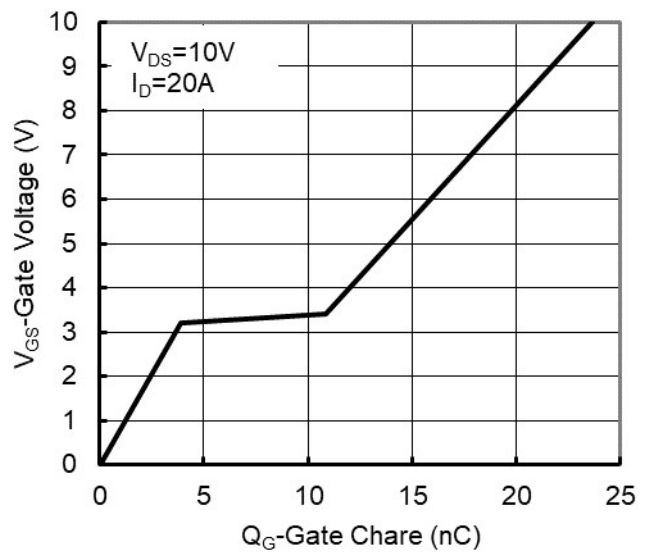


Figure6. Gate Charge



# YJQ13N03A

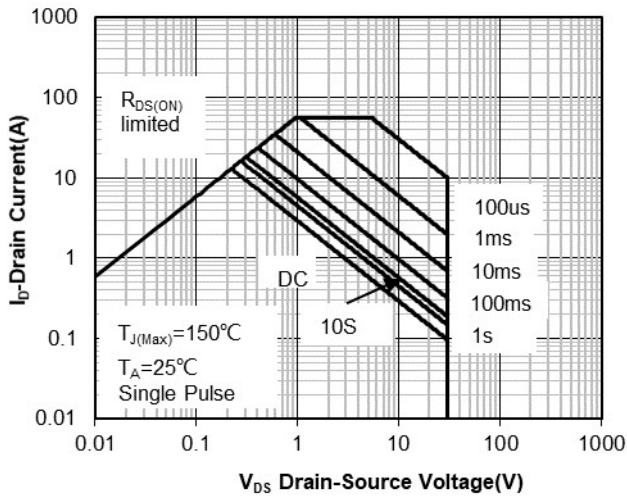


Figure7. Safe Operation Area

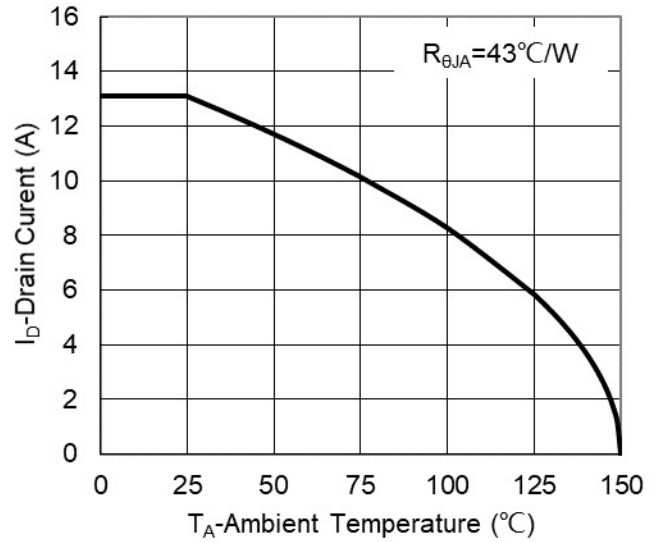


Figure8. Maximum Continuous Drain Current vs Ambient Temperature

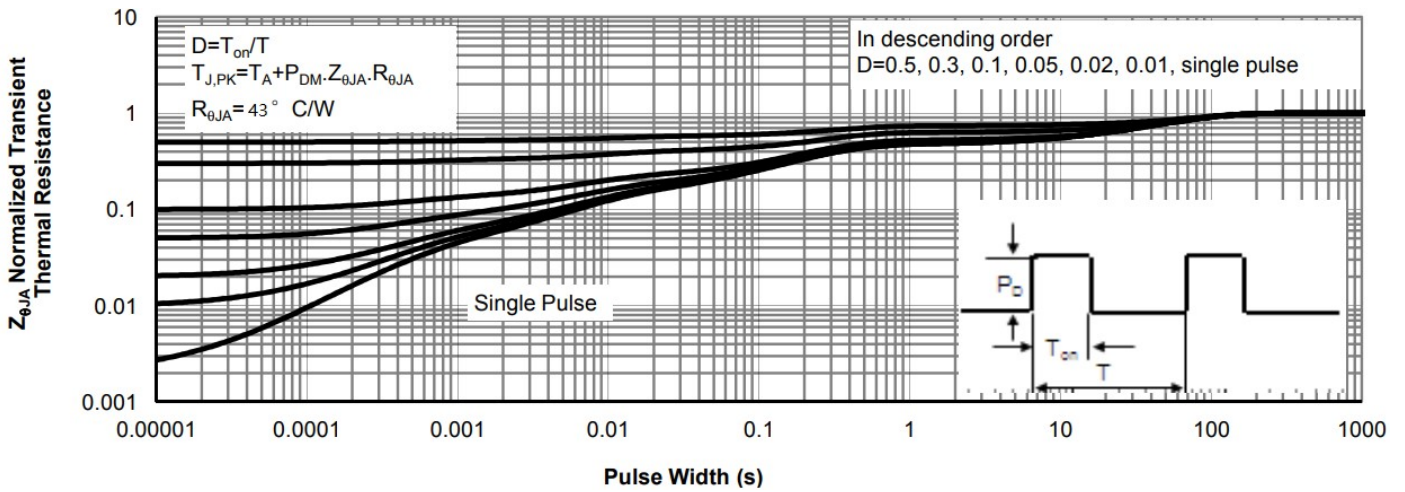
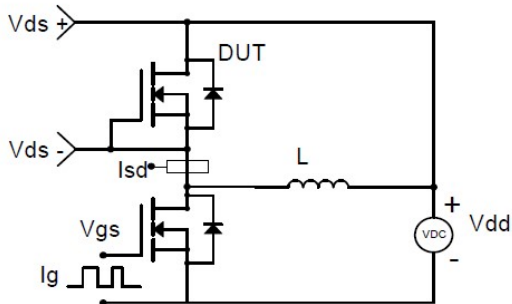


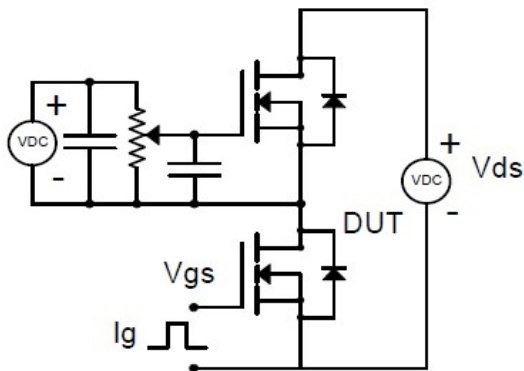
Figure9. Normalized Maximum Transient Thermal Impedance



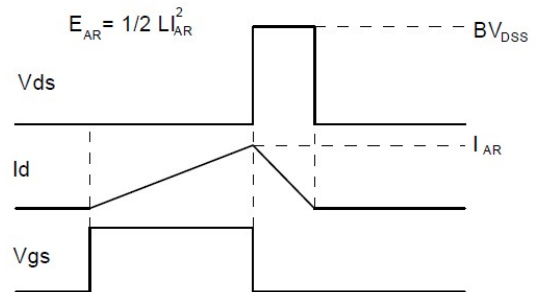
**Resistive Switching Test Circuit & Waveforms**



**Diode Recovery Test Circuit & Waveforms**



**Gate Charge Test Circuit & Waveform**

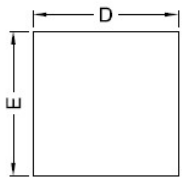


**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**

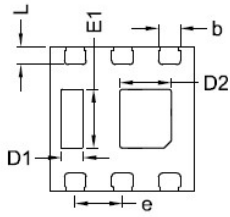


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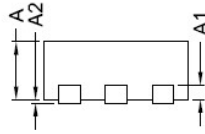
## DFN2x2-6L(0.8mm) Package information



Top View  
正面视图

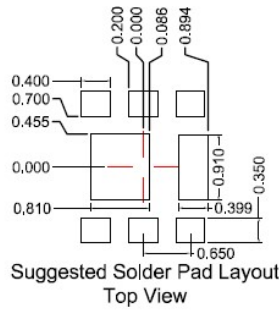


Bottom View  
背面视图



Side View  
侧面视图

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	1.90	2.00	2.10
E	1.90	2.00	2.10
A	0.70	0.80	0.90
A1	0.20 BSC		
A2			0.10
D1	0.20	0.30	0.40
D2	0.61	0.71	0.81
E1	0.71	0.81	0.91
L	0.15	0.25	0.35
b	0.20	0.30	0.40
e	0.65 BSC		



Note:

1. Controlling dimension: in millimeters.
2. General tolerance:  $\pm 0.10$ mm.
3. The pad layout is for reference purposes only.



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